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Transformerless topologies for grid-connected single-phase photovoltaic inverters

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ABSTRACT

In order to improve the efficiency and reduce the cost of a photovoltaic system, the use of transformerless photovoltaic inverters is an alternative of increasing interest. However, this topology needs to be studied in detail, as it presents some problems related to the galvanic connection between the grid and the photovoltaic generator (e.g. efficiency degradation and safety problems).

In this paper, a review of grid-connected single-phase photovoltaic inverters based on transformerless topologies has been carried out. On the one hand, some alternatives based on classical topologies have been presented. On the other hand, alternatives based on multi-level inverter topologies have been studied, showing up that no leakage current is generated in comparison to classical topologies.

Contents

1. Introduction

The renewable energy sources, in particular those of photovoltaic origin [1], have experimented a great development in recent years mainly due to the growing concern about global warming, and the grants given by the governments to these kind of technologies [2,3].

Power processing of renewable energy sources is carried out by means of power converters, with some issues like efficiency and cost as key factors. In the particular case of grid-connected photovoltaic inverters, most of the power converter topologies use a transformer operating at low or at high frequency, which provides galvanic isolation between photovoltaic panels and electrical grid. Low frequency transformers are big, heavy and expensive, and

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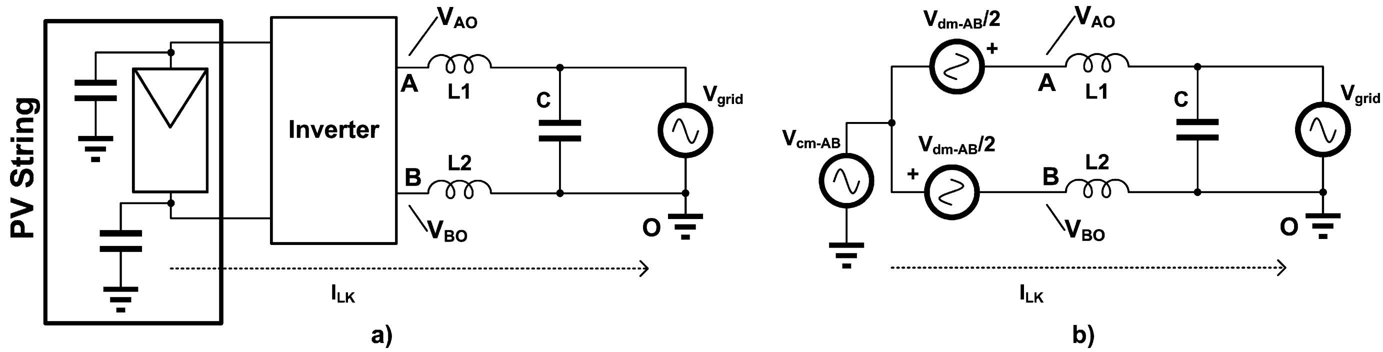


Fig. 1. (a) Common mode current and parasitic capacitance and (b) photovoltaic system model.

introduce additional losses in the system. The size of the isolating transformer may be significantly reduced by using a two stage topology in which the transformer operates at high frequency [4], this approach reduces the efficiency because at least two cascaded power converters are needed. Because of that, a large number of inverters based on transformerless topologies [5,6] have been proposed in the last few years, resulting in cheaper, more compact and more efficient power processing systems [7]. In addition, when using transformerless inverters some technique to measure the isolation resistance and the residual current must be used, which makes the transformerless inverters even safer than the inverters with transformer [8].

Regarding the size of grid connected power inverters, a change of paradigm has been observed in the last few years [9,10]. Large central inverters of power above 100 kW are being substituted by small size inverters that processes the energy supplied by one string or a small group of strings. Following this approach, the maximum power point tracking of large photovoltaic groups of panels can be improved, as they could be exposed to very different solar radiation levels [11]. In this context, the use of single-phase inverters up to 5 kW is of a great interest.

For the aforementioned reasons a significant number of small-power topologies have been proposed to implement grid connected single-phase transformerless inverters [12]. In this kind of inverters there is no galvanic isolation between photovoltaic panels and the grid, so that some problems can appear that need a special care, like common mode voltages and leakage currents across the photovoltaic panels, due to the fact that a non-negligible parasitic capacitance exists between photovoltaic cells and the installation ground, which can reach very high values under certain operating conditions (e.g. humidity, dust, or installation mode). Typical values of this capacitance vary between 50 and 150 nF/kWp for crystalline-Silicon cells and values up to 1 μF/kWp for thin-film cells.

2. The common mode voltage problem

The commutation of the inverter switches can produce an alternating common mode voltage in the panel poles, which may induce a capacitive leakage current [13,14], as shown in Fig. 1(a) and (b).

The value of the common mode voltage can be estimated following (1), where the mismatch between the values of the grid filter inductors, L_1 and L_2, is taken into account, and play an important role in the common mode voltage problem [15].

$$V_{\text{CM-AB}} = \frac{(V_{\text{AO}} + V_{\text{BO}})}{2} + \frac{(V_{\text{AO}} - V_{\text{BO}}) \cdot (L_2 - L_1)}{(2 \cdot (L_1 + L_2))} \quad (1)$$

Because of the effect of both, the parasitic capacitance of the panels and the inverter common mode voltage, a leakage current to the ground appears, which may produce serious problems in photovoltaic power plants (e.g. actuation of the protections, efficiency degradation, safety problems, additional distortion of the grid current and electromagnetic compatibility problems) [7,16–20].

When unipolar PWM modulation is used in the transformerless full H-bridge inverter, a high frequency common mode voltage is applied to the photovoltaic panels, so that a non-negligible leakage current appears, as shown in Fig. 2, where the test conditions have been choice to be as follows; Output power: 5 kW, grid voltage: 230 V/50 Hz, filter LC: 2 × 850 μH/12 μF, switching frequency: 10 kHz, ground resistance: 1 Ω, leakage capacitance: 2 × 140 nF.

Furthermore, it has been detected additional problems associated to leakage current in emerging cells technologies. When using back-contact photovoltaic cells operated at high voltage values, leakage current forms negative charges on the cells front surface, affecting recombination mechanism and reducing the cells efficiency. Fortunately, this is a reversible effect if the power photovoltaic inverter is designed to tie the negative photovoltaic string pole to ground, thus generating a negative voltage gradient which avoids this phenomenon [7]. In the case of amorphous-Silicon thin-film cells (a-Si) and cadmium telluride (CdTe), if moisture condenses inside the module and negative voltages to ground exist, an irreversible corrosive process can be started at the TCO (Transparent Conducting Oxide) [7,21]. This phenomenon leads to a reduction in the efficiency and, consequently, to a shorter photovoltaic modules life. To prevent this, it is mandatory to avoid condensation inside the photovoltaic module by hermetically sealing the modules border. However, it is difficult to guarantee the

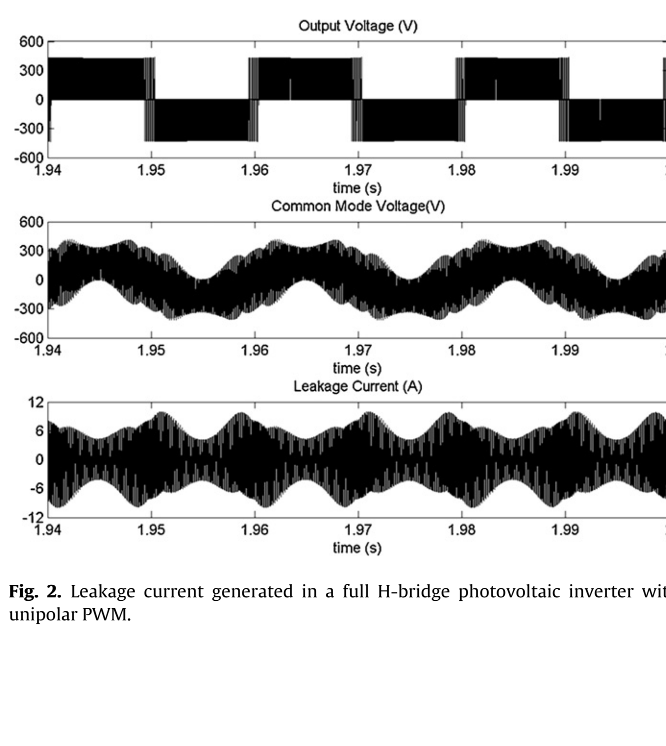


Fig. 2. Leakage current generated in a full H-bridge photovoltaic inverter with unipolar PWM.

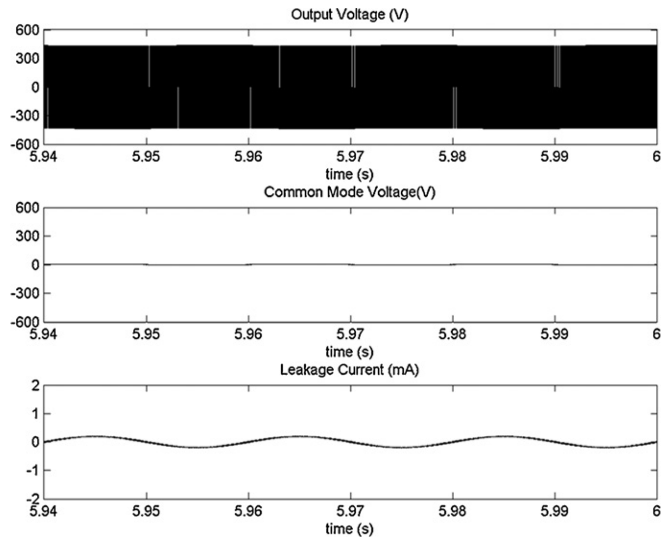


Fig. 3. Leakage current generated in a half H-bridge photovoltaic inverter.

functionality of this system over the years. Another highly effective measure is to ground the negative pole of the panels, avoiding the corrosion process due to the electric field orientation.

Research on transformerless inverters focuses on finding topologies which have a low leakage current, while trying to keep or to improve the performance of the classical topologies [22], e.g. the half H-bridge topology, which presents a very low leakage current since neutral is connected to the midpoint of the input voltage, as depicted in Fig. 3, where the test conditions have been choice to be the same as in Fig. 2.

This paper presents a review of topologies that have been previously proposed to implement single-phase transformerless photovoltaic inverters, by emphasizing in some aspects of interest like the common-mode voltages applied to photovoltaic panels, the quality of the generated current and the number and characteristics of the semiconductors used in each topology.

3. Power converters derived from bridge topologies

These inverters are based on full H-bridge and half H-bridge structures, and have been widely studied in the literature. In this section, it will be analyzed the following transformerless topologies: full H-bridge with both unipolar and bipolar modulation, half H-bridge, HERIC topology, H5 topology and half H-bridge with an additional generation control circuit.

3.1. Full H-bridge

The most widely used topology in grid-connected photovoltaic inverters is the full H-bridge. It is build up by 4 transistors, which are connected as shown in Fig. 4. Due to the fact that a large number of commercial inverters use this topology in combination with a low frequency transformer it is interesting to study its application to transformerless inverters.

The most common modulation used in this topology is unipolar PWM, because it presents a number of advantages in comparison to bipolar modulation (e.g. lower current ripple at high frequencies, better efficiency or lower electromagnetic interferences emission) [23]. However, when unipolar PWM modulation is used in the transformerless full H-bridge inverter, a high frequency common mode voltage of amplitude $V_{dc}/2$ is applied to the photovoltaic panels, so that a non-negligible leakage current appears because of the photovoltaic panels parasitic capacitance. This reason advises

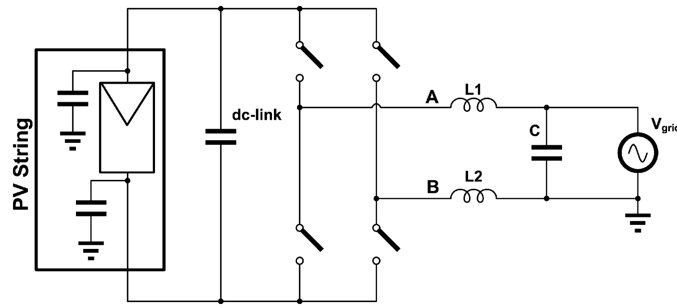


Fig. 4. The full H-bridge topology.

against using this kind of modulation in transformerless inverters [24].

To solve the problem of the leakage current in the full H-bridge photovoltaic inverter, the Bipolar PWM modulation can be used. This modulation eliminates the high frequency components of the common-mode voltage applied to the panels [8], thus the common mode voltage only has the low frequency component of the first harmonic, so that a reduced leakage current results [13,14,25]. However, to limit the leakage current peak value, it is critical a good synchronization among the gate signals of the bridge transistors. Otherwise, the leakage current could significantly increase [26]. Consequently, this topology is not considered to be a good alternative to implement transformerless photovoltaic inverters, even if the bipolar PWM modulation is used [27].

3.2. Half H-bridge

The half H-bridge topology is formed by 2 transistors and a capacitive divider connected to the photovoltaic module, as shown in Fig. 5. The connection of the grid neutral wire to the capacitive divider midpoint ensures an almost constant common mode voltage, thus preventing leakage current through the parasitic capacitance of the photovoltaic module [28].

Despite the lower cost and simplicity of this converter compared to the H-bridge topology (mainly due to fact that the half H-bridge uses half of the semiconductors than the H-bridge) [29], this topology is rarely used in practice, because of some drawbacks difficult to solve (e.g. the output waveform has only two levels, the output current is highly distorted and causes high electromagnetic interference emissions, and the switches have to support double the voltage compared to the full H-bridge topology) [15,28] thus requiring higher blocking voltage power transistors, which increases the switching losses.

In order to improve the behavior of the half H-bridge, several variants of this topology have been presented in the literature as interesting alternatives for transformerless inverters. The most important ones are shown next.

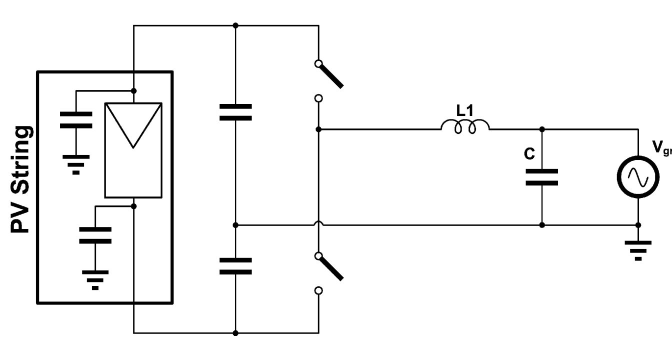


Fig. 5. The Half H-bridge inverter topology.

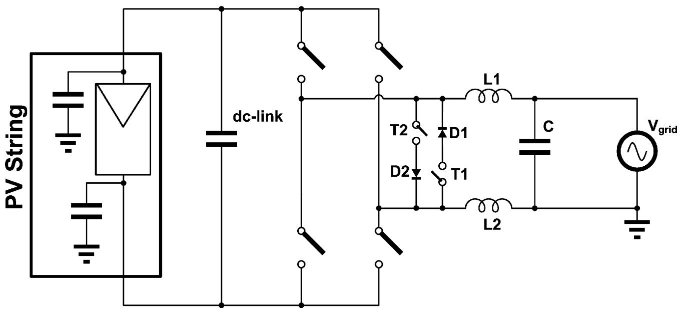


Fig. 6. The HERIC topology.

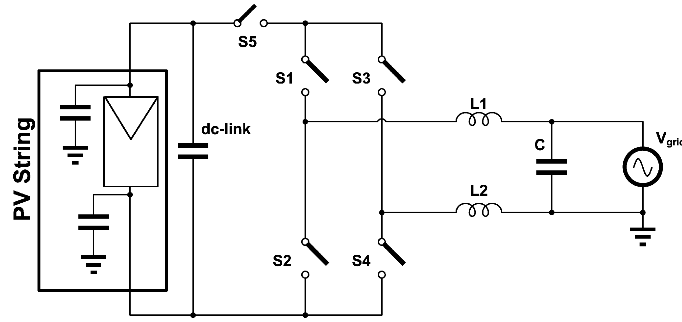


Fig. 7. The H5 topology.

3.3. High efficient and reliable inverter concept (HERIC)

This topology combines the advantages of the unipolar PWM modulation with a reduced leakage current and a high efficiency, being the topology implemented in some commercial inverters [8,24], especially those from Sunways.

As stated in previous sections, it is interesting to use a 3 level output voltage transformerless inverter to connect the photovoltaic panels to the electrical grid. However, the results shown in Fig. 2 using a full h-bridge have shown that this arrangement introduces a high frequency ripple in the photovoltaic poles, which causes a non-negligible leakage current to flow through the parasitic capacitance of the panels into the ground. To avoid the leakage current while maintaining the 3 level output voltage, a new topology based on the full H-bridge inverter has been developed and patented [30], known by the acronym HERIC.

In the HERIC topology a couple of branches are added in parallel with the output filter, as shown in Fig. 6. These additional branches switch at the electrical grid frequency, so that T1 is in the on-state in the positive half-cycle and in the off-state in the negative half-cycle, while T2 is the on-state in the negative half-cycle and in the off-state in the positive half-cycle. This allow the diodes D1 and D2 to work as a free-wheeling diodes in the positive and the negative half-cycles, respectively, thus preventing the output current to flow through the diodes of the full H-bridge. The described feature is responsible for isolating the photovoltaic panel from the electrical grid, as well as for obtaining the third level, i.e. 0 V, in the output voltage of the inverter, since the same one remains short-circuited when D1 or D2 conduct. The HERIC topology allows the photovoltaic panel to remain at a floating voltage to ground, thus achieving a practically constant common mode voltage [8].

Moreover, it is possible to improve efficiency as compared with a conventional H-bridge, due to the fact that during free-wheeling periods current does not flow through bridge semiconductors. This characteristic is of great use when the inverter is operated at light load conditions [6,8,31].

The main drawback of HERIC topology is the high number of switches, which leads to a greater complexity of the converter compared to the conventional full H-bridge topology.

3.4. The H5 topology

This topology only needs an additional transistor compared to the full-bridge, and that is the reason for its name. The H5 topology is patented by SMA [32], which is considered as one of the worldwide leading manufacturers of photovoltaic inverters, and it is based on the same concept as the HERIC topology, i.e. to disconnect the photovoltaic panels from the grid during current freewheeling periods, which prevents the voltage to ground of panel poles from switching frequency ripple, thus having an almost constant common mode voltage.

In Fig. 7 it is shown the H5 topology, that uses a full-bridge consisting of the four switches S1, S2, S3 and S4, and the DC-bypass S5 switch. The switches S1 and S2 are operated at grid frequency, whereas S3, S4 and S5 are operated at high frequency. During current free-wheeling period, S5 is open, disconnecting photovoltaic panels from the inverter full H-bridge. The free-wheeling path is closed by the transistor of S1 and the inverse diode of S3 for the positive half-cycle of the electrical grid and by the transistor of S3 and the inverse diode of S1 for the negative half-cycle.

The use of the H5 transformerless inverter topology makes possible to obtain a high efficiency [33], particularly at partial load. It needs only one additional transistor in comparison with the full H-bridge topology. However, as the transistor is in series with the full H-bridge inverter [16], the conduction losses may increase if the semiconductor choice is not optimum.

Nowadays, some commercial inverters use this topology [24], especially those from the proprietary of the patent, being a valid alternative to implement transformerless photovoltaic inverters.

3.5. Half H-bridge with generation control circuit (GCC)

Half bridge with GCC [34] is based on a half-bridge inverter with two more additional transistors, which makes it possible the independent maximum power point tracking of the photovoltaic strings [35]. A schematic of this topology is depicted in Fig. 8. In this figure it is possible to identify both, the GCC circuit, composed of the switches S1 and S2 and the inductor L1, and the half H-bridge circuit, consisting of the switches S3 and S4 and the inductor L2.

The GCC is a classical buck-boost chopper [36] that uses the middle point and the negative pole of the DC-link capacitor bank as the input and positive pole and the middle point of the DC-link capac-

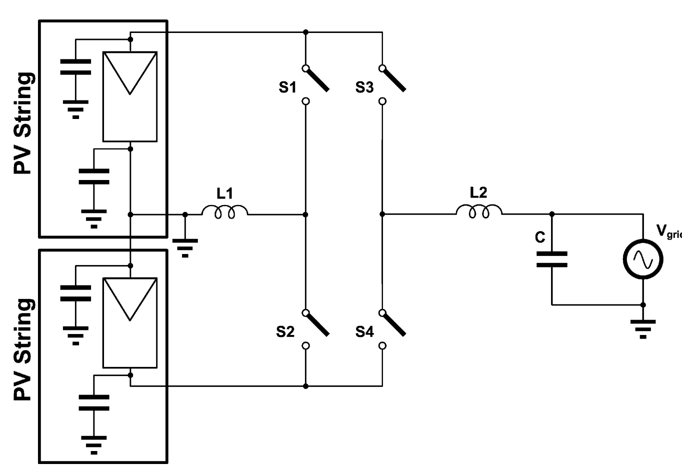


Fig. 8. The half-bridge with generation control circuit topology.

itor bank as the output, thus allowing to share the load current between the different strings.

In spite of the fact that there exist other alternatives than the GCC to perform the independent maximum power point tracking of a several photovoltaic panels, this topology is of a great interest when a pair of strings are used, since it needs the same component count as a full H-bridge, i.e. 4 transistors and 2 inductors, while retaining the common-mode voltage performance of a half H-bridge converter, thus ensuring a low common mode current. Furthermore, the dc/dc of the GCC switches only the power difference between the photovoltaic strings, reducing the overall power losses.

It is worth pointing out that the performance of the inverter is comparable to the performance of the half H-bridge, and that the drawbacks are the same, i.e. higher current ripple, higher power losses and higher electromagnetic interferences than the full H-bridge. However, by using the GCC it is possible to improve the performance of the photovoltaic panels, due to the fact that the maximum power point of both panels can be tracked independently [11] which is important in those installations where different strings are subjected to different installation conditions (e.g. different orientation, partial shadows or even a small difference in the number of panels of each string).

4. Inverters based on multilevel topologies

The multilevel topologies are based on a special arrangement of the semiconductors and passive components of the inverter in such a way that a three or more discrete DC voltage levels are obtained at the power converter output. Although these topologies have been widely used in high power applications [37], it has not been considered so far as an alternative to the standard topologies used in small-power transformerless inverters, mainly due to the cost of the extra required power diodes and transistors. However, thanks to the cost reduction of semiconductors [38,39], the multilevel topologies are being recently applied to the development of small-power transformerless inverters.

It is important pointing out that these kind of converters should overcome two important limitations. On the one hand, a reduction on the number of sensed magnitudes should be accomplished. On the other hand, the building blocks of the multilevel converters should be designed to reduce the parasitic inductance [40]. To overcome these limitations, the manufacturers of semiconductors are developing power modules which integrate basic multilevel structures [41].

The following transformerless multilevel topologies are presented below: cascaded H-bridge (CHB), NPC half-bridge, flying capacitor (FC), a variant of the NPC half-bridge, the Conergy-NPC and the active-NPC (aNPC).

4.1. Cascaded H-bridge (CHB)

The simplest multilevel structure consists in connecting H-bridge cells in series by its AC-side, while using a different photovoltaic panel for each DC-link [42]. A schematic of a two stage CHB multilevel inverter with a second order output filter is shown in Fig. 9.

It should be pointed out that this multilevel topology requires as many isolated power sources as H-bridge power stages, which is considered a problem when it is used in classical power electronics applications (e.g. high power motor drives). However, photovoltaic modules meet this requirement, which in turn has made the CHB topology an interesting choice for the photovoltaic power inverter design process [43].

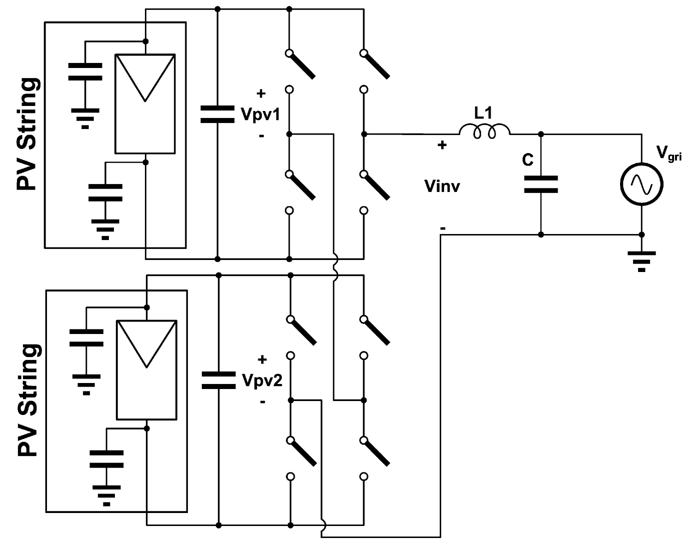


Fig. 9. The cascaded H-bridge multilevel inverter.

One of the most interesting feature in this topology is the ability to boost the inverter AC side voltage enough to inject current into the grid without using neither a transformer nor an additional boost converter [5,25,44], due to the fact that as much modules as desired can be stacked in series, thus increasing the number of output voltage levels (e.g. in Fig. 9, a maximum of Vpv1 + Vpv2 is obtained at the inverter output voltage, Vinv). In fact, this characteristic has motivated the study of different maximum power point tracking strategies which enables the independent control of each group of photovoltaic modules [45,46], while controlling the current injected into the electric grid. It is worth pointing out that some works have exploited this modular structure to work even with damaged power cells [47,48], thus increasing the reliability of the system.

Finally, it should be noted that the number of semiconductors needed would affect the cost and the reliability, and that the leakage current can be high, depending on the number of cells connected in series.

4.2. NPC half-bridge

The NPC half-bridge is the single-phase revision of the multilevel topology used in high-power motor-drive applications [49], which has been recently proposed as an alternative topology to be used in photovoltaic inverters design. It consists of a branch with 4 transistors and 2 clamping diodes, as shown in Fig. 10. The diodes offer a free-wheeling path for the output current that causes the 0 V output voltage state [8].

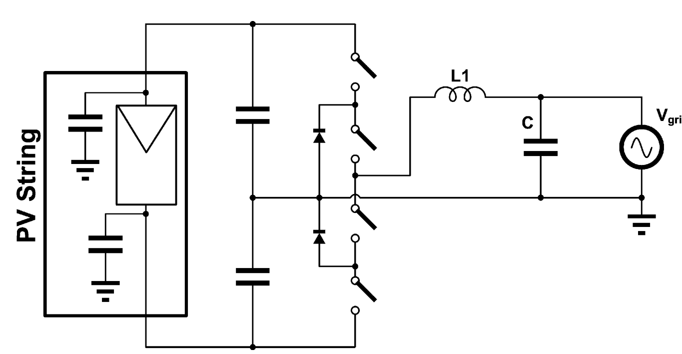


Fig. 10. The NPC half-bridge inverter.

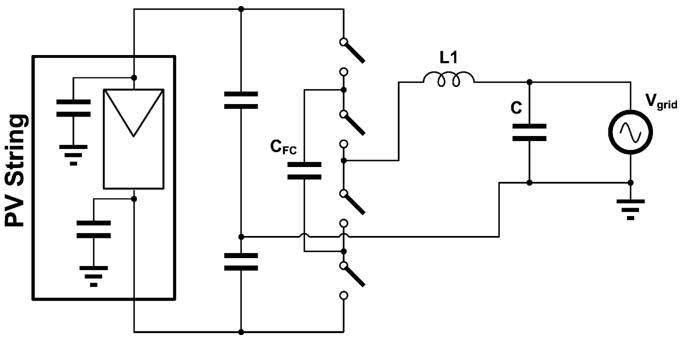


Fig. 11. The FC inverter.

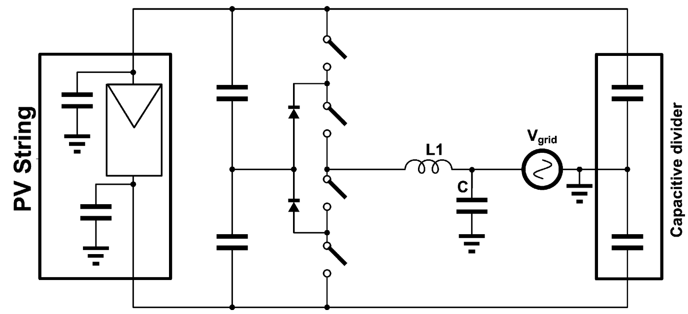


Fig. 12. The NPC half-bridge with capacitive divider.

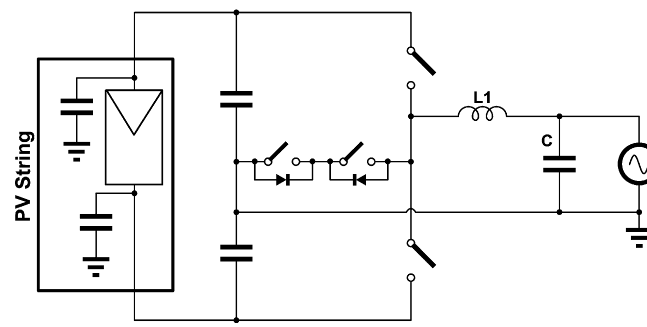


Fig. 13. The Conergy NPC inverter.

On the one hand, the NPC half-bridge topology works in a similar way that the half-bridge, but it has better efficiency, less current ripple [15] and a constant common mode voltage, thus preventing the leakage currents. On the other hand, the NPC topology has a performance similar to the full-bridge topology with unipolar PWM modulation, i.e. 3 output inverter voltage levels, and a similar voltage derivative. Consequently, the output filter and the performance of the converter are similar to a unipolar PWM modulated full-bridge [14].

The main drawbacks of this topology are listed next. It requires a large number of power semiconductors, a high capacity bank of capacitors [5,25] and a high input voltage, which doubles the full-bridge input voltage [24]. Another important problem is the transient overvoltage that takes place at the internal transistors, due to the absence of capacitors in parallel [50]. Nevertheless, this problem can be solved by using a snubber circuit. Furthermore, power losses are not uniformly distributed over all the semiconductors [51].

Finally, it is worth pointing out that this alternative is about 15% cheaper than cascaded H-bridge (CHB) or flying-capacitor (FC) topologies [52], as well as a robust and simple one, so that it can be found in some commercial transformerless inverters. Moreover, some manufacturers of semiconductors offer power modules with an integrated complete NPC branch.

4.3. Flying capacitor (FC)

The structure and performance of the flying capacitor topology is similar to the NPC topology described above [53,54], so that it presents a very low leakage current. The floating capacitor CFC depicted in Fig. 11 replaces the clamping diodes used in the NPC half-bridge topology, and provides the third level at output voltage, i.e. the 0 V level.

To avoid an undesired overvoltage at the transistors during the startup, a special circuit to pre-charge the floating capacitor will be required [55]. In addition, the voltage of the floating capacitor has to be controlled in order to maintain its value at a given reference, so the FC control strategy is more complicated than the NPC control strategy [5,56]. However, a simple technique that uses the inductive output impedance of the inverter can be used when there are few output levels [57]. This technique is based on the redundant switches states of the inverter [58,59].

An interesting feature of the FC inverter is the fault-tolerant operation that can be obtained when the number of levels is high enough. This operation allows the inverter to continue working even if a transistor or a floating capacitor is damaged [60,61].

4.4. NPC half-bridge with a capacitive divider

This topology, adds a capacitive divider to the aforementioned NPC half-bridge [15], thus avoiding the direct connection of the neutral wire to the midpoint of the dc-link, as shown in Fig. 12. This ensures that the voltage of the strings poles remains constant through the additional capacitive divider, hence obtaining a reduced leakage current.

It is important pointing out that if neutral wire is connected directly to the midpoint of the dc-link the use of high-accuracy sensors is necessary to ensure that no dc-current is injected to the electrical so that the cost and complexity of the whole system is increased. In the NPC half-bridge with a capacitive divider topology, the capacitors integrates the dc component of the output current over the time, thereby facilitating its detection with less-accurate voltage sensors and, therefore, with a lower cost despite the two additional high current capacitors. It should be noted that the rest of advantages and drawbacks of the proposed topology are the same as the ones derived from the NPC half-bridge topology.

4.5. Conergy NPC

The Conergy NPC is another variant of the NPC half-bridge that has been developed and patented by Conergy [62]. In Fig. 13 is shown the basic schematic of the topology, which consists of a

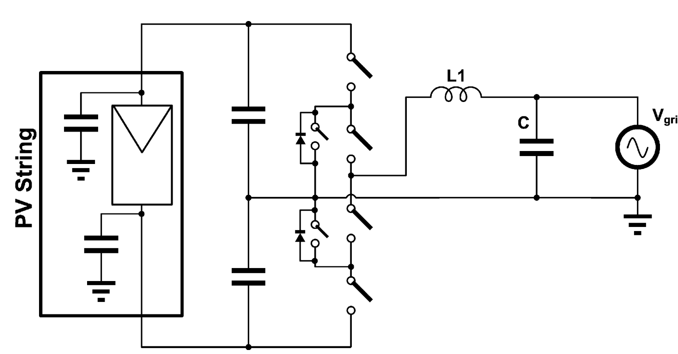


Fig. 14. The active NPC inverter.

Table 1
Comparison of the several proposed topologies.

	H-bridge (unipolar PWM)	H-bridge (bipolar PWM)	Half-bridge	HERIC topology	H5 topology	Half-bridge with GCC	Cascaded H-bridge (n cells)	NPC half-bridge	Flying capacitor (FC)	NPC variant	Conergy NPC	Active NPC (ANPC)
Input capacitors	1	1	2	1	1	2	n	2	3	4	2	2
Input capacitance	Low	Low	High	Low	Low	Medium	Very high	High	High	High	High	High
Switches	4	4	2	6	5	4	$4n$	4	4	4	4	6
Diodes	0	0	0	2	0	0	0	2	0	2	0	0
Transistors voltage	400 V	400 V	800 V	400 V	400 V	800 V	400 V/n	400 V	400 V	400 V	400 V	400 V
Output voltage levels	3	2	2	3	3	2	$2n-1$	3	3	3	3	3
First harmonic	2fsw	fsw	fsw	2fsw	2fw	fsw	2$n$fsw	2fsw	2fsw	2fsw	2fsw	2fsw
Electromagnetic Interferences	Low	High	High	Low	Low	High	Very low	Low	Low	Low	Low	Low
Number of MPPTs	1	1	1	1	1	2	n	1	1	1	1	1
Leakage current	High	Low	Very low	Very low	Very low	Very low	Medium	Very low	Very low	Very low	Very low	Very low

half-bridge inverter and a branch that can apply 0 V to the output voltage.

The characteristics of this topology are similar to those of the NPC half-bridge, but it offers a higher efficiency, making it suitable for low-power applications [63].

4.6. Active NPC (ANPC)

It is possible to substitute the clamping diodes of the NPC inverter by power transistors with anti-parallel diodes, which lead to the topology shown in Fig. 14. This topology is called active NPC (ANPC) and its main feature lies in the control of the current path during the free-wheeling periods [63,64], which lets the distribution of losses to be improved [65–67], thus loading uniformly the power transistors, and increasing the maximum output power of the converter [49,51]. However, sometimes it could be cheaper to select a higher maximum current NPC topology [68], especially in low-power applications.

5. Characteristics of transformerless PV inverters at a glance

In order to get a better performance understanding of the several topologies presented up until now, it is interesting to compare them by previously defining the next key items:

- *Number of input capacitors and capacitance*: The input capacitors are used to supply the AC component of the input current. In some topologies more than one capacitor (or more than one bank of capacitors) is necessary and, therefore, the design of the dc-link is more complicated. In some topologies the frequency of the input current is low and, therefore, the input capacitance necessary can reach high values.
- *Power semiconductors*: It is important to use the minimum number of power switches, as it affects directly to the cost of the converter. The voltage rating of a semiconductor usually affects its power losses and, therefore, it is interesting to implement topologies with a low voltage rating in the switches.
- *Output voltage*: A good output voltage quality implies a good output current quality, with a low current harmonic content which is easy to filter out. This implies that the topologies that are capable of obtaining a three level output voltage have better performance and lower electromagnetic emission than those that have only two level output voltage.
- *Number of MPPTs*: A photovoltaic inverter has to be able to control its input voltage to manage the power obtained from the photovoltaic modules. Some topologies can control more than one input voltage, so it is possible to track several maximum power points, hence improving the performance under different isolation conditions.
- *Leakage current*: As explained previously in the introduction, it is mandatory to reduce the leakage current in the transformerless inverters.

In Table 1 it is shown the comparative between the proposed topologies by using the items previously defined.

6. Conclusions

In this paper a review of transformerless topologies for single-phase photovoltaic inverters is presented. On one hand, alternatives based on classical topologies, derived from half-bridge and full-bridge are widely studied. On the other hand, topologies based on multi-level inverters are presented, as they are under development. Main problem of transformerless topologies is the

fluctuating voltage to ground at input poles. Two methods for solving this problem are presented: disconnecting the photovoltaic panels from the grid during free-wheeling periods, or connecting the neutral wire to one pole of the photovoltaic panels.

In the half-bridge topologies the input current has a component of 50 Hz, while in the full-bridge topologies the frequency of this component is 100 Hz. Hence, the full-bridge topologies require less input capacitance than the half-bridge ones. Thus, a full-bridge converter might have a better reliability and a lower cost than a half-bridge one.

The CHB topology uses the lowest voltage rating switches, so it can achieve a high efficiency; however, it needs a large number of switches. On the contrary, the half-bridge topology needs only 2 switches, but they need to block the highest voltage.

In order to obtain a good ratio between performance and converter cost, it is desirable to obtain a three-level output voltage. The full-bridge topology and some multilevel half-bridge topologies allow the converter to obtain three level output voltage. Furthermore, the CHB topology can produce a higher number of output voltage levels.

The generation control circuit can be used with the half-bridge topology, thus controlling two input voltages. If the CHB topology is used, then a higher number of voltages can be controlled at the input of the converter.

The HERIC and H5 topologies present a very low leakage current if the synchronization between the gate signals is correctly adjusted. In addition, it is worth pointing out that all the half-bridge topologies with the neutral connected to the midpoint of the input voltage presents pretty low leakage current.

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